Abstract

Using the SUMMiT V™ process, the team designed a mechanical binary counting device (µCounter) to mimic the interactions that take place inside an equivalent electrical analog, commonly produced as a microchip. Using these unique components, a binary counter that comes preprogrammed was developed. It is a full six bit binary counter, and is programmed to reset at 60 (or 111100) instead of resetting at a typical 6-bit binary overflow of 64 (or 111111). This counter was designed to bring new concepts and designs into a MEMS device utilizing strengths of the SUMMiT V™ process, and expanding on its standard components library.

Objectives

- Demonstrate data flow through a mechanical circuit with analogs of common electronic components; the resistor, capacitor, diode, transistor, and memory.
- Introduce variations of standard SUMMiT V ™ components for consideration.

Introduction

Inspired by the Digi-Comp II mechanical computers of the 1960's, the 6-bit µCounter illustrates simple digital logic by linking modified gears to create a mechanical accumulator which sums individual bits. Like the Digi-Comp II, the µCounter enables viewers to follow the flow of bits through a system. However the µCounter provides a user-friendly display mechanism for viewing the binary value of each bit in the register (Figure 4).

Current visualization tools that help people to understand electrical flow are generally presented with diagrams or through computer simulations. In contrast, with this counter observers can actually see the flow of data through the system. The use of mechanical processing systems has been phased out over the years, and now most systems, even the simple ones are purely electrical. These micromechanical components and this counter design make it possible to produce EMP resistant processors for simple and secure processing.

Using the one-of-a-kind tools and abilities of the SUMMiT V™ process, including: the five unique layers, extremely flat CMP (chemical mechanical polishing) surfaces, and the uniform spacing between layers allowed the counter to be compact and accurate. The benefits of the ultra planar SUMMiT V™ allowed for unique structures to be designed around standard components without worry of binding or time-intensive design iterations.

Description

The µCounter utilizes standard SUMMiT V components, and modifications thereof, to produce analogs of well-known electronic devices – the capacitor, diode, resistor, and transistor. Linking these mechanical equivalents creates functional subsystems - the accumulator, memory, and

operator. When integrated as a whole each component plays a part in counting input waveform pulses and displaying the results. Much like the Digi-Comp II that inspired its design, the µCounter permits observers to trace data as it flows through the mechanical circuit.

The following list briefly describes unique components integrated into the design:

a. Input – Periodic signal sufficient to rotate the TRA by one tooth. The built-in gearing ratio counts the rotation of 15 teeth as one bit. Therefore, if the device were operated by a continuous 15 Hz signal, the register would accumulate 60 bits in one minute.
b. Transistor – Switches input between one of two outputs; the accumulator or display. Constructed of a 15 tooth MMPOLY3 half gear anchored to a 30 tooth MMPOLY1&2 gear, the transistor either updates a binary readout display or passes the bit along the accumulator.
c. Display – Provides a binary readout of registered bit values by rotating a MMPOLY1&2 gear marked with a "0" and "1" beneath a window cut into the MMPOLY3 layer.
d. Resistor – Prevents gears from freely spinning while the transistor disengages. In terms of today's processor speeds, the 15 Hz input signal may seem negligible. However, this relatively slow rate translates into 30 revolutions per minute (RPM) on a 30 tooth gear. Since the SUMMiT V™ process produces features of such fine tolerances, the affect of frictional force on a spinning gear about its hub appears trivial. Therefore, when a gear spinning at 30 RPM is suddenly disengaged, it could continue to spin with relatively little friction to stop it. The resistor prevents this from happening by introducing a gear with an internal ratcheting system. This can provide resistance by requiring each of the fifteen flexible arms of the design to overcome approximately three microns of linear displacement each. The amount of resistive force can be varied to fit design needs using the number, angle, or width of the internal arms.
e. Diode – Ratcheting gear only allowing spin in one direction.
f. Capacitor – Stores energy as tension in a spring. As the four most significant bits in the 6-bit register accumulate, the memory rack shifts toward the input thereby tensioning the spring capacitor, saving the energy for later use during the reset operation.
g. Cache – Stores value of the accumulator's four most significant bits.
h. Operator – Gearing assembly configured to reset accumulator once count reaches sixty.
i. Accumulator – Bit counter assembly. Comprised of five transistors, four diodes, a resistor and various gears, the accumulator counts bits and updates registry displays.

The design was started by laying out an achievable data flow diagram (Figure 1), which aided in the construction of certain specialized parts. The data flow we chose allows for six bits to be represented and can be modified to be reset at any value before the overflow (64). This device provided enough components to test the design as well as represent the time in seconds or minutes as a binary readout. Although the binary number system was chosen for the device, other base scales such as $base_5$ or $base_6$ (both of which were used to simplify the reset circuit).

The first issue that came to the table was that the resistance to the gears rotation was too small to keep the bit paths aligned. To solve this issue, a 15 tooth latch (Figure 5) was created to act as a resistor. This allowed the flow through but provided enough resistance to stop any residual rotation after the bit path was cut off. In order to read the direction of the pipeline: whether it was ready to pass a bit (on or 1), or if it was ready to receive a bit (off or 0). This was done by connecting a display gear directly to the transistor gear (Figure 3).

To solve the issue of programming, and how to actuate the transistors, a mechanical way to store data had to be designed. To do this, we first needed to translate the representation of the bit from rotational movement. Using a linear rack, a memory cache was created which, after receiving a bit of data would disconnect from the system (Figure 7). This bit would later be used to reset the transistor. However, this posed yet another problem: what would latch the memory into place, and what would store the power needed to activate the release of the memory?

This issue was solved by creating a capacitive device that would store enough energy to reset the transistor to any desired position. The capacitor is a simple coiled spring that gathers the spring energy during compression (Figure 8). For the spring, the poly 1 & 2 laminate was utilized because of their extra thickness. The latch mechanism covers the spring, and was created on MMPOLY3 and anchored directly to the gear. The latch covers the spring and keeps it contained in the capacitor gear. The arresting pawl was created outside of the gear allowing actuation of the pawl to release the capacitor. To make sure the pawl was always engaged with the teeth of the latch, the capacitor was covered with a MMPOLY4 structure.

At this point of development, it can count with our six binary digits. It will also store energy to release into the transistors to set their value. The next design step was to create something that could release the capacitor pawl, this however posed a challenge. The pawl needed to travel up to three microns to allow the capacitor latch to ratchet correctly. To solve the travel distance issue a guide was created that would allow the pawl to travel on its own, but would also allow the guide to pull the pawl from the latch teeth. The guide transfers its 35° of rotation into liner movement in order to pull the pawl free from the latch. The guide needed to actuate, but the linear travel for data through the system needed to move towards the TRA. For this, a linear rack would connect all capacitors to a single reset circuit, although each could easily be actuated individually with another counter. The linear travel from the linear rack connects the pawl guide (Figure 9). The system design used allows the latches to be released smoothly and the release mechanism to be

controlled and not bind. At this point all the transistors required to reset were programmed. Now, creating a timer circuit was required.

The timer circuit used a $base_5$ and a $base_6$ transistor, connecting them resulted in an output every 30 bits. To reset it at 60, a system to pull the linear reset rack every 2 bits was created. Using all of the SUMMiT V™ layers, a double lobe camshaft was developed to actuate the rail every time the counter hit 60. The camshaft amplifies the movement by using a spring driven lever to help the cam follower on the camshaft. This system linked these two systems without transferring a bit between them, which performs the same task as a relay.

At this point, the device contains only the resistor, capacitor, relay, transistor, and register, but when the capacitors energy is released into the transistor there must be a way to keep energy from flowing in the opposite direction. This is where the complex, one-of-a-kind system was created: a diode that would allow the data to travel through the system as usual until the capacitor releases its' energy back into the system as negative rotation. The diode allows the meshing gears to spin without transferring their energy in one direction, while allowing smooth passage of energy in the other.

Using the resistor and two of the special diode gears a mechanical diode was created for the use of driving gears. Using the unique built-in hub construction of the SUMMiT V™ process, a double hub was designed that allowed two gears to spin independently on the same hub structure. This hub was the center point for the diode now the two independent gears needed to be connected in one direction but independent in the other direction, for this, a complex ratchet was required. Utilizing all five layers of SUMMiT V™ a ratchet was developed that worked in the conventional way, but was mounted backwards due to the hub design. Instead of having the center point of the ratchet connected to the bottom gear, and the outer teeth connected to the top gear, a third layer was used. The ratchet was connected on poly 3 and directly anchored on the outside to the poly 1/2 gear below it. The center and arresting pawls where connected to the center hub and to a poly 4 layer that attached outside of the ratchet. This allowed for both a gear and ratchet to be on poly 3 as well as having poly 4 supporting the teeth, while connecting them to the ratchet.

The counter was designed to bring new concepts and designs into a MEMS product utilizing SUMMiT V™ strengths and expanding on their usefulness. The counter currently represents a few ideas; the most useful and potentially expandable idea would be: creating mechanical versions of electrical chips to protect essential systems from EMP effects. Other uses include using the counter as a way to create ROM (Read Only Memory) at mechanical level. Other uses include utilizing it as learning device (using a MEMS platform). The counter should be able to count to 60 and reset every time. However, with so many new designs in a single system the potential for issues is possible.

SUMMiT V™ strengths where utilized to the fullest extent for this counter: the five unique layers, extremely flat CMP surface finish, and the uniform spacing between layers ensured that the gears would mesh correctly and that all supporting structures would maintain their critical dimensions. The SUMMiT V™ processes unique MMPOLY1&2 laminate and pin-joint cut were essential in creating the double hub design for the resistor while allowing the gears to have controlled rotation. The ultra planer surfaces due to the CMP steps are vital for every action of the binary counter - from the rotation of gears and the movement of the linear racks to maintaining tolerances in the ratchets and springs used. The tools included with SUMMiT V™ are essential for any MEMS project. The trace and gear generators, as well as the tested, standardized component libraries help make simple designs a reality in a matter of seconds. The three-dimensional modeling tools, DRC checker, and cross-section viewer make visualizing and editing designs fast and easy.

Pending fabrication and testing, modifications to the fundamental design could enable performing simple arithmetic. For instance, reconfiguring the operator might permit summing independent bit streams. Extending this concept further, simple processing systems may evolve providing mechanical processors resistant to the effects of Electro Magnetic Pulses (EMP). For the time being, the μCounter's best feature remains capturing a viewer's attention, allowing them to witness data as it flows through a mechanical system.

Summary

Using the SUMMiT V™ process we designed a device to represent the interactions that take place inside an ordinary electrical adding circuit. Mechanical versions of the capacitor, relay, diode, transistor, and memory were created. The one-of-a-kind tools and abilities of the SUMMiT V™ process including the five unique layers, extremely flat CMP (chemical mechanical polishing) surfacing, and the uniform spacing between layers allows our counter to be compact and accurate. The benefits of the ultra planar MEMS SUMMiT V™ allowed for unique structures to be designed around standard components. It is possible to expand and improve these designs to produce EMP resistant devices for simple and secure processing. The binary counter brings many important innovations to the SUMMiT V™ process, including the double independent hub and linear hinged lever.

Appendix

Figure 1 - Data Flow Diagram

The memory, capacitors, transistors and operator enable programming the µCounter.

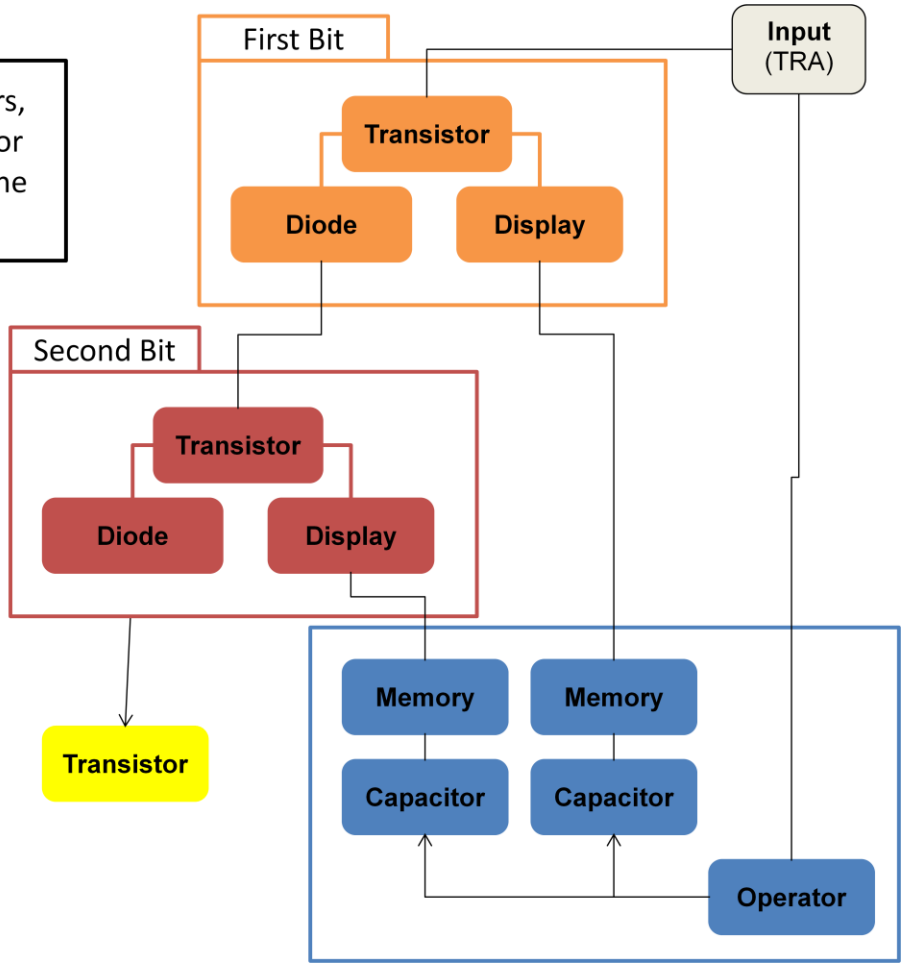


Figure 2 - Design Subsystems

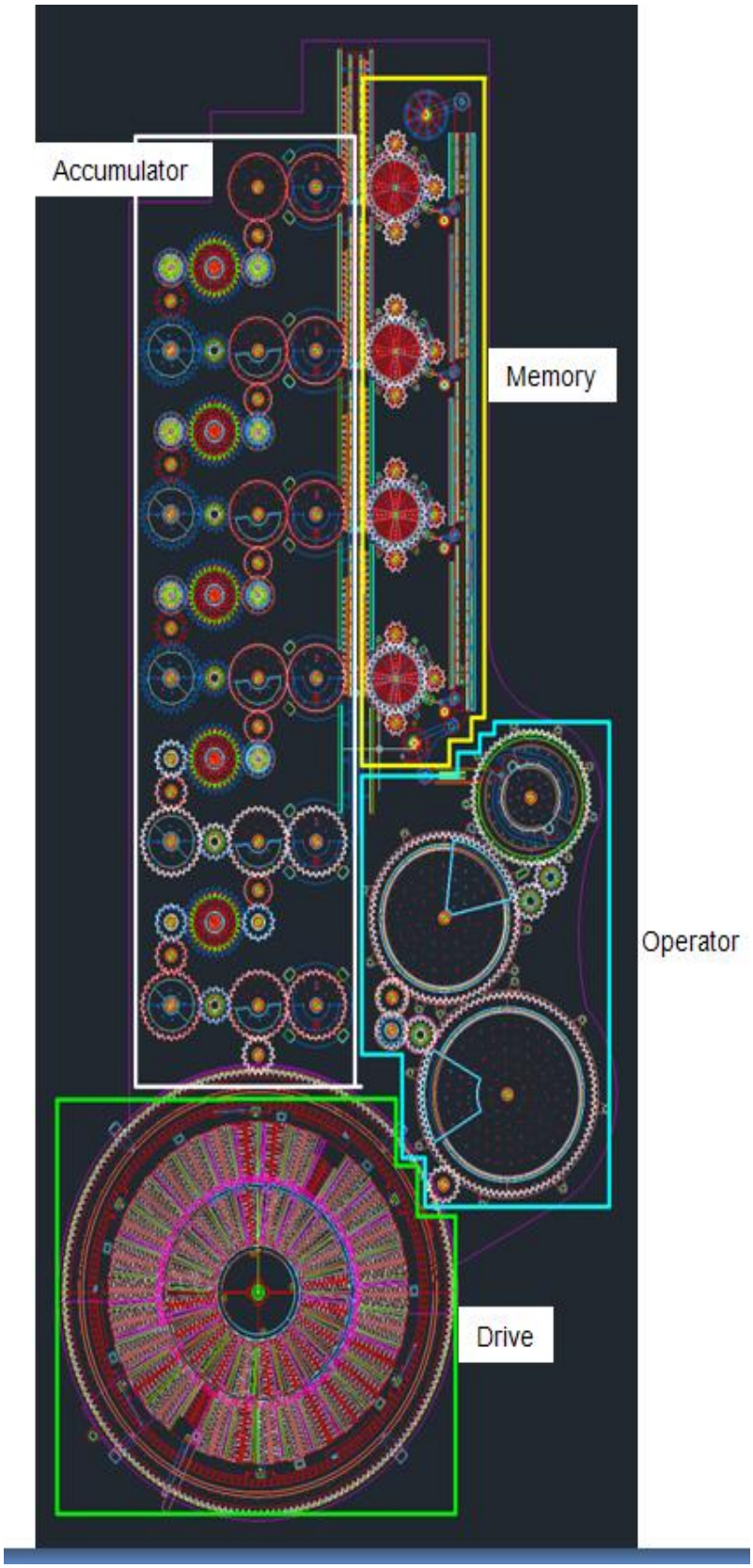
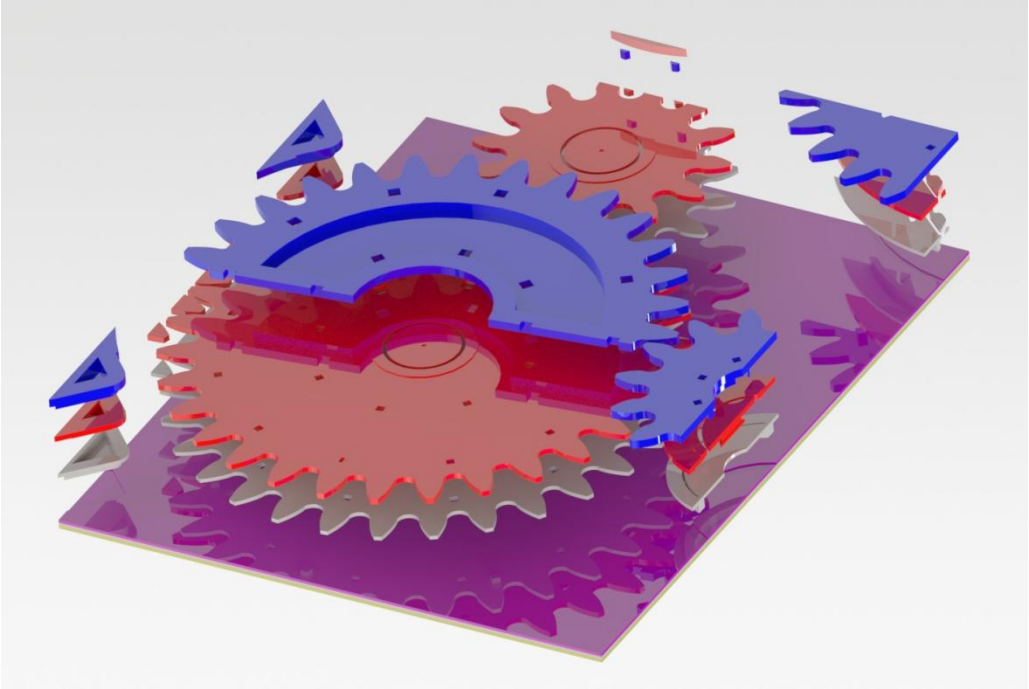


Figure 3 - Transistors



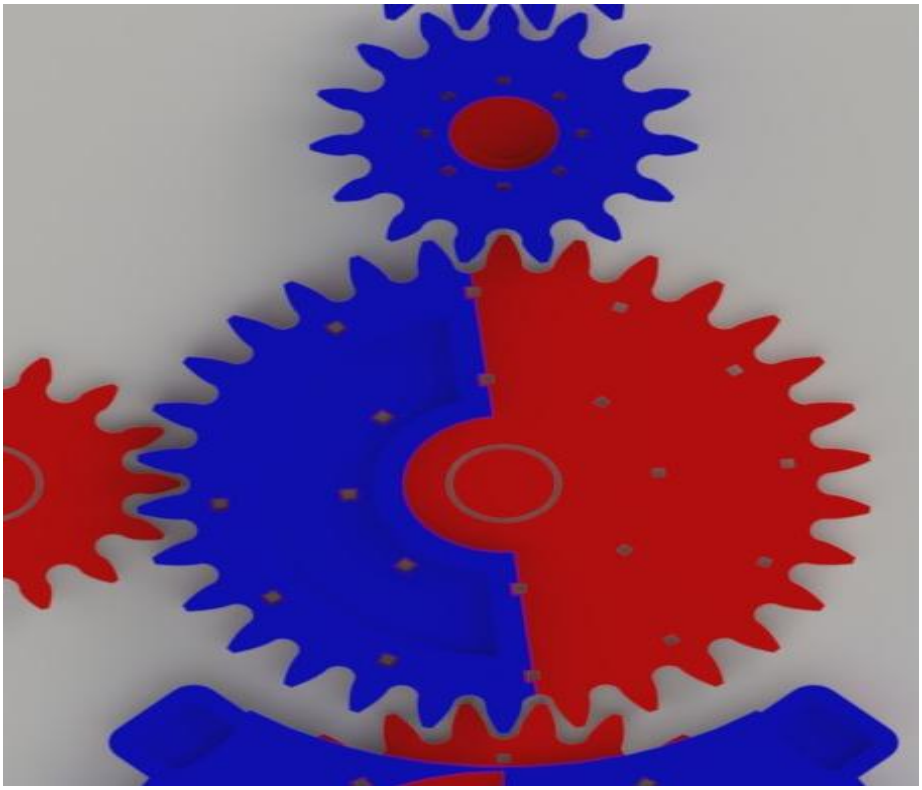


Figure 4 - Binary Display

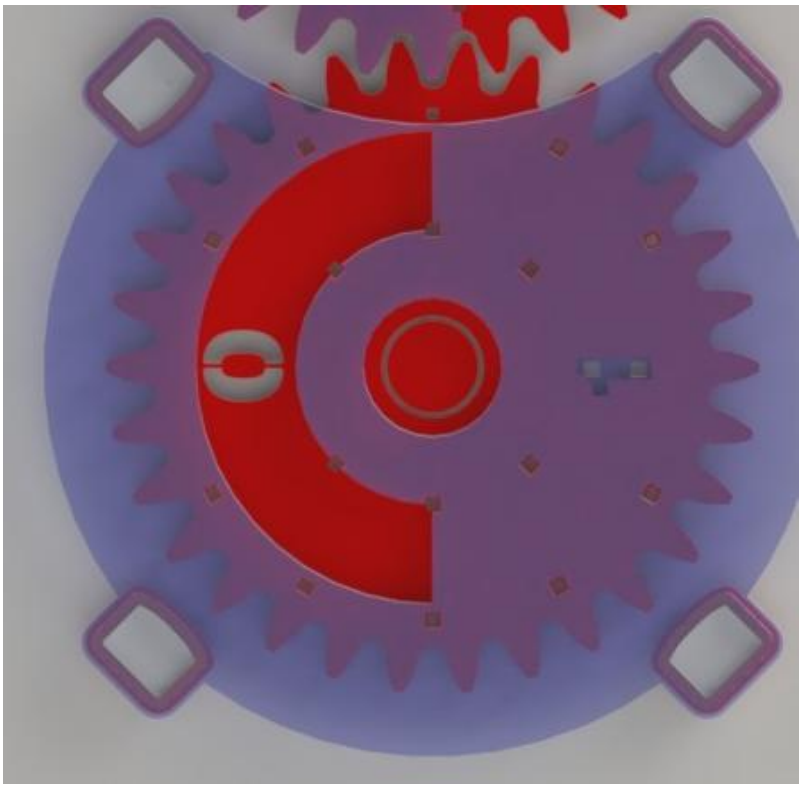
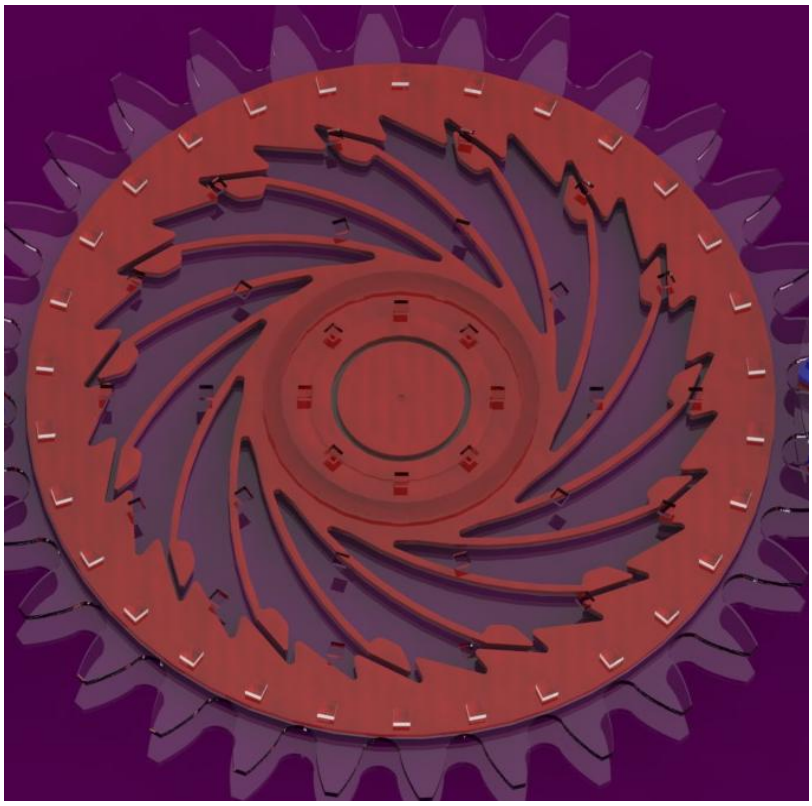


Figure 5 - Resistors



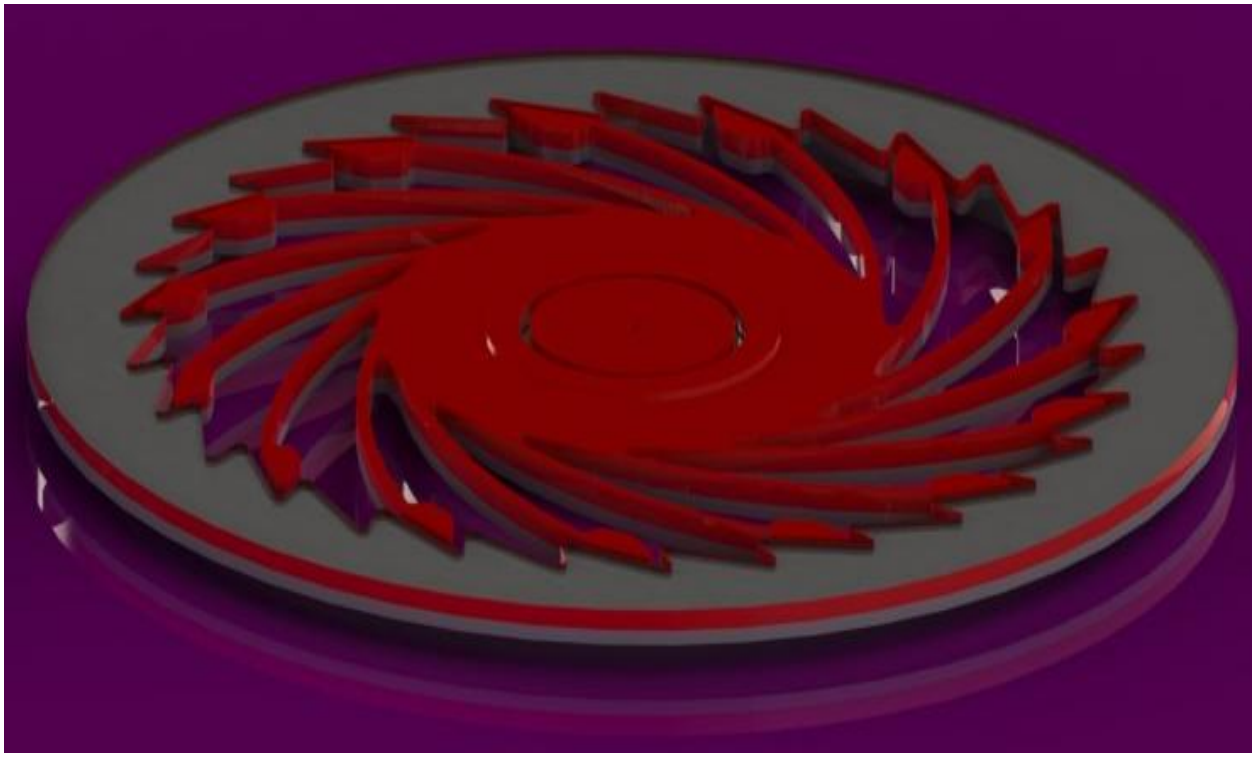


Figure 6 - Diodes

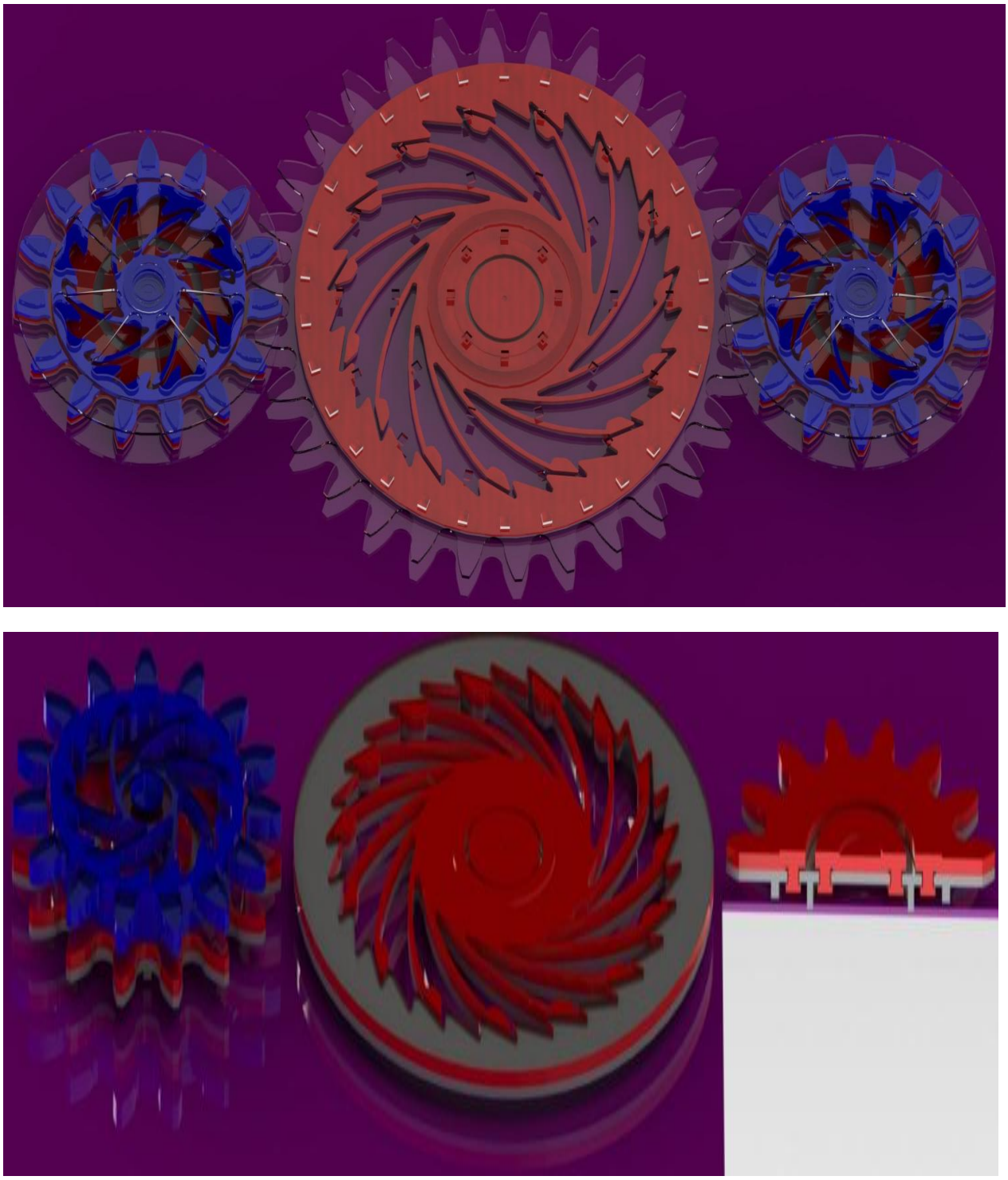


Figure 7 - Memory

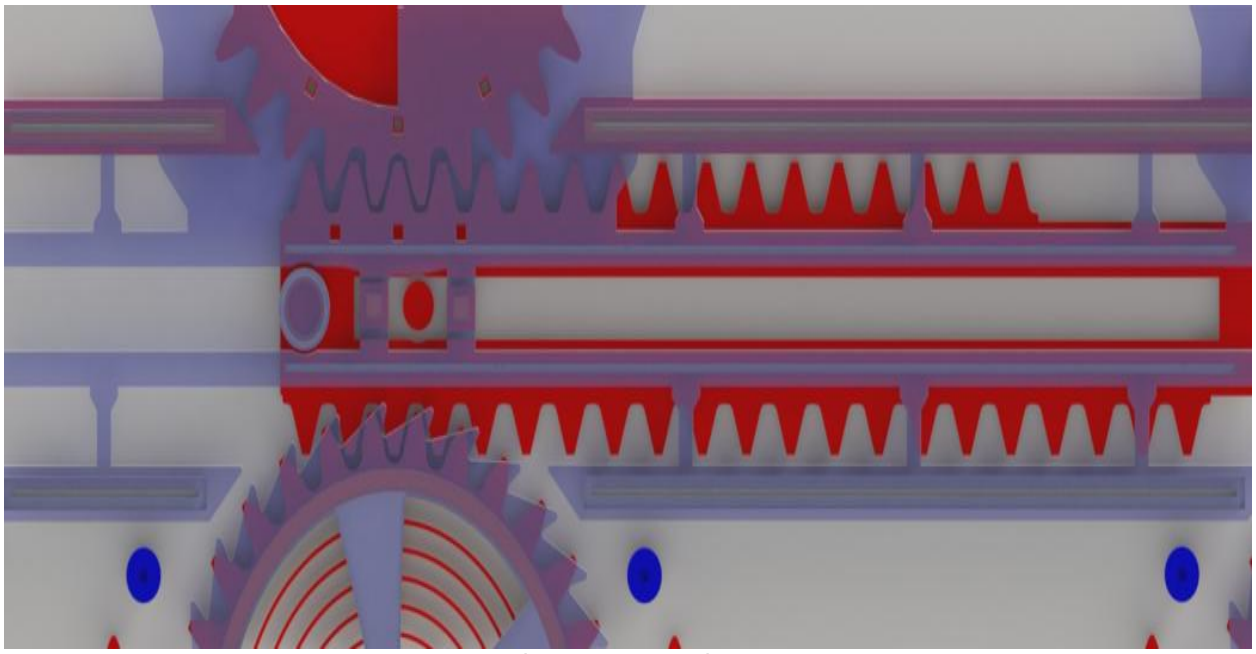


Figure 8 - Capacitor

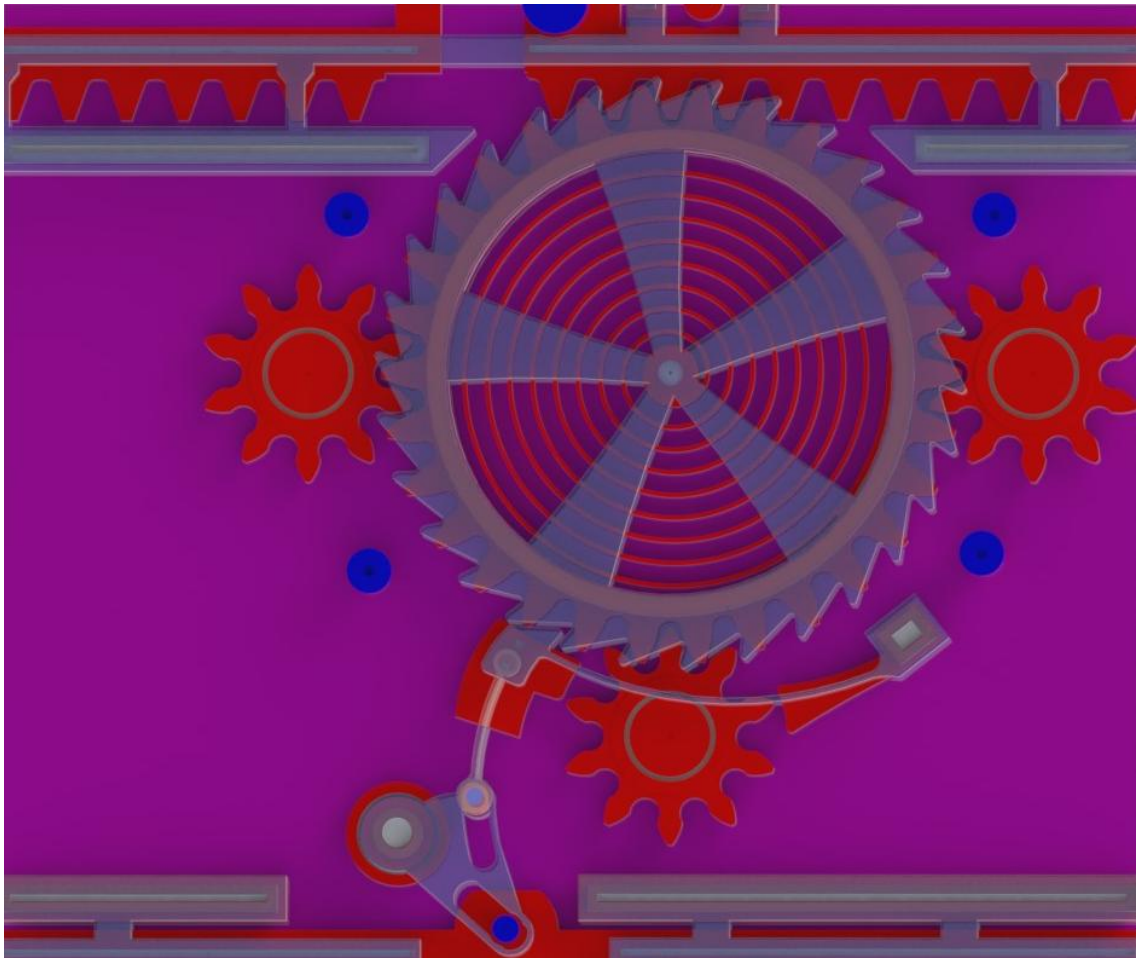


Figure 9 - Cam Assembly